Experiment Number -01

PEE-452/PCS-405 Microprocessors Lab
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OBJECT

To study 8085 based Microprocessor System.

APPRATUS REQUIRED

8085 Microprocessor trainer kit

THEORY

Architecture of 8085 Microprocessor

The Intel 8085 is an 8-bit microprocessor produced by Intel and introduced in 1976. It is a software-binary compatible with the more-famous Intel 8080 with only two minor instructions added to support its added interrupt and serial input/output features. However, it requires less support circuitry, allowing simpler and less expensive microcomputer systems to be built.

It consists of five essential blocks.

i. Arithmetic Logic Section
ii. Register Section
iii. The Interrupt Control Section
iv. Serial I/O Section
v. The Timing And Control Unit

Intel 8085

An Intel 8085AH processor.

Produced	From 1975 to 1990s
Common manufacturer(s)	Intel and several others
Max. CPU clock rate	3, 5 and 6 MHz
Min. feature size	3 µm
Instruction set	80
Transistors	6,500
Predecessor	Intel 8080
Successor	Intel 8086
Package(s)	40-pin DIP

1. **General purpose register**
   It is an 8 bit register i.e. B,C,D,E,H,L. The combination of 8 bit register is known as register pair, which can hold 16 bit data. The HL pair is used to act as memory pointer is accessible to program.
2. **Accumulator**
   It is an 8 bit register which hold one of the data to be processed by ALU and stored the result of the operation.

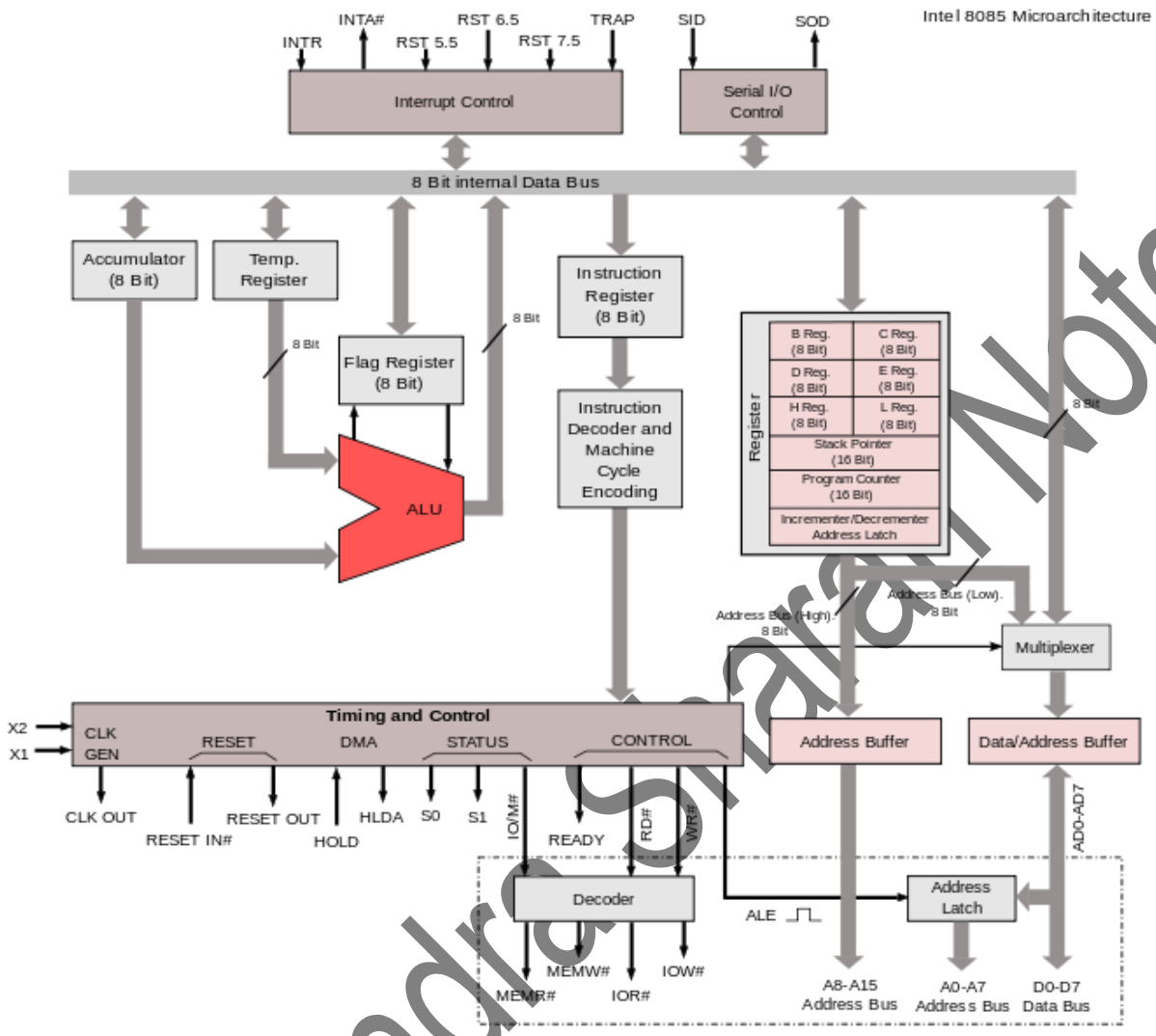

Fig. 1.1 Architecture of 8085 Microprocessor

3. **Program counter (PC)**

   It is a 16 bit pointer which maintain the address of a byte entered to line stack.

4. **Stack pointer (Sp)**

   It is a 16 bit special purpose register which is used to hold line memory address for line next instruction to be executed.

5. **Arithmetic and logical unit**

   It carries out arithmetic and logical operation by 8 bit address it uses the accumulator content as input the ALU result is stored back into accumulator.

6. **Temporary register**

   It is an 8 bit register associated with ALU hold data, entering an operation, used by the microprocessor and not accessible to programs.

7. **Flags**

Flag register is a group of fire, individual flip flops line content of line flag register will change after execution of arithmetic and logic operation. The line states flags are

a. Carry flag (C) **c.** Zero flag (Z) **e.** Sign flag (S)

b. Parity flag (P) **d.** Auxiliary carry flag (AC)

8. Timing and control unit

Synchronous all microprocessor, operation with the clock and generator and control signal from it necessary to communicate between controller and peripherals.

9. Instruction register and decoder

Instruction is fetched from line memory and stored in line instruction register decoder the stored information.

10. Register Array

These are used to store 8 bit data during execution of some instruction.

PIN DESCRIPTION

Address Bus

11. The pins Ao – A15 denote the address bus.

12. They are used for most significant bit

Address / Data Bus

- AD0 – AD7 constitutes the address / Data bus
- These pins are used for least significant bit

ALE : (Address Latch Enable)

- The signal goes high during the first clock cycle and enables the lower order address bits.

IO / M

- This distinguishes whether the address is for memory or input.
- When this pins go high, the address is for an I/O device.

S0 – S1

- S0 and S1 are status signal which provides different status and functions.

RD

- This is an active low signal
- This signal is used to control READ operation of the microprocessor.

WR

- WR is also an active low signal
- Controls the write operation of the microprocessor.

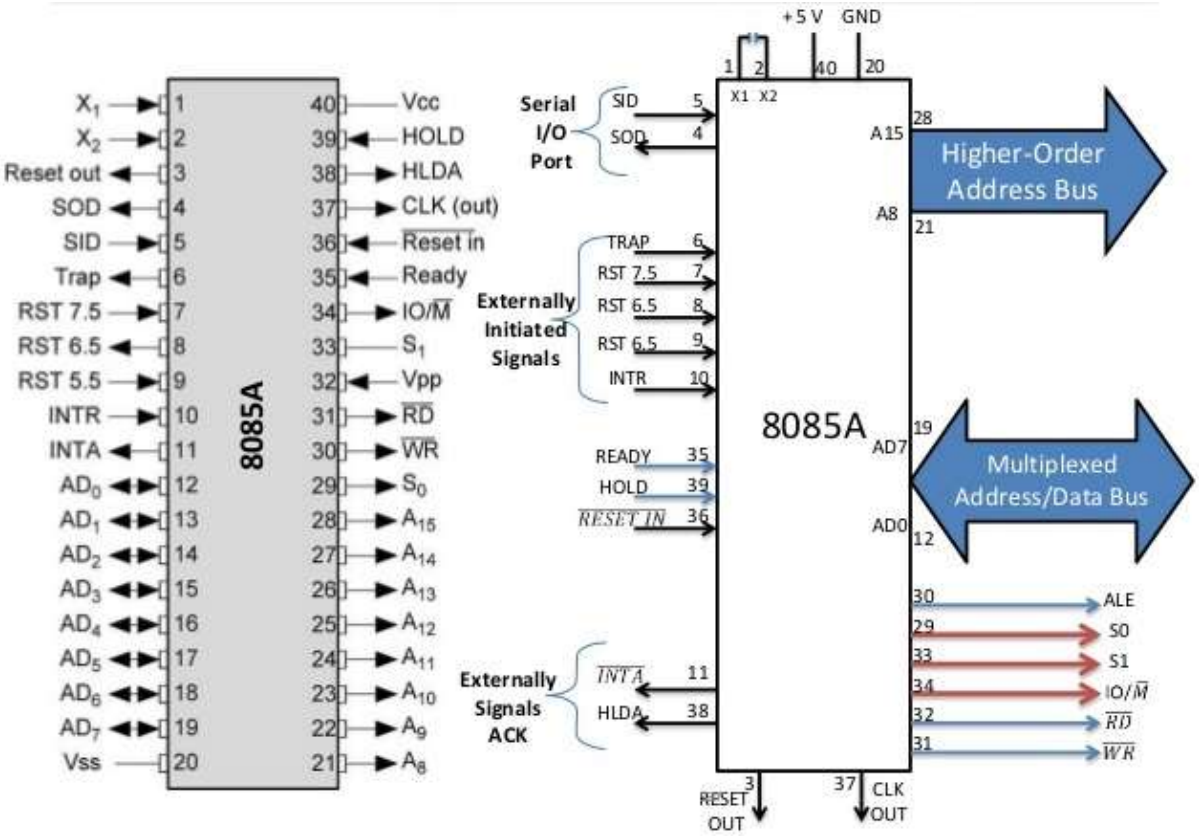

Fig 1.2 Pin Diagram of 8085A Microprocessor

HOLD

- This indicates if any other device is requesting the use of address and data bus.

HLDA

- HLDA is the acknowledgement signal for HOLD
- It indicates whether the hold signal is received or not.

INTR

- INTE is an interrupt request signal
- IT can be enabled or disabled by using software

INTA

- Whenever the microprocessor receives interrupt signal
- It has to be acknowledged.

RST 5.5, 6.5, 7.5

- These are nothing but the restart interrupts
- They insert an internal restart junction automatically.

TRAP

- Trap is the only non-maskable interrupt
- It cannot be enabled (or) disabled using program.

RESET IN

- This pin resets the program counter to 0 to 1 and results interrupt enable and HLDA flip flops.

X1, X2

- These are the terminals which are connected to external oscillator to produce the necessary and suitable clock operation.

SID

- This pin provides serial input data

SOD

- This pin provides serial output data

VCC and VSS

- VCC is +5V supply pin
- VSS is ground pin

SPECIFICATIONS

1. **Processors**

   Intel 8085 at E144 MHz clock

2. **Memory**

Monitor RAM:	0000 – IEFF
EPROM Expansion:	2000 – 3FFF's
	0000 – FFF
System RAM:	4000 – 5FFF
Monitor data area	4100 – 5FFF
RAM Expansion	6000 – BFFF

3. **Input / Output**

   Parallel: A8 TTL input timer with 2 number of 32-55 only input timer available in µ-85 EBI.

   Serial: Only one number RS 232-C, Compatible, crucial interface using 8281A

   Timer: 3 channel -16 bit programmable units, using 8253 channel '0' used for no band late. Clock generator. Channel '1' is used for single stopping used program.

   Display: 6 digit – 7 segment LED display with filter 4 digit for adder display and 2 digit for data display.

   Key board: 21 keys, soft keyboard including common keys and hexa decimal keys.

   RES: Reset keys allow to terminate any present activity and retain to µ - 85 its on initialize state.

INT: Maskable interrupt connect to CPU's RST 7.5 interrupt

DEC: Decrement the adder by 1

EXEC: Execute line particular value after selecting address through go command.

NEXT: Increment the address by 1 and then display its content.

SYSTEM POWER CONSUMPTION

Micro BSEB2	MICRO SSEB
+5V @ 1Amp	+5V@ 800 mA
+12V @ 200 mA	
- 12V @ 100 mA	

POWER SUPPLY SPECIFICATION

MICRO SSEM

230V, AC @ 80 Hz +5V @ 600 mA

IC's Used

8085 - 8 bit µp

8253 - Programmable internal timer

8255 - Programmable peripheral interface

8279 - Programmable key boards / display interface

8251 - Programmable communication interface

2764 - 8 KV VV EPROM

6264 - 8K STATIC PROM

7414 - Hex inverter

7432 - Quad 21/p OR GATE

7409 - Quad 21/p AND GATE

7400 - NAND Gate

7404 - Dual D-FF

74373 - Octal 'D' Latch

74139 - Dual 2 to 4 line decoder

74138 - 3 to 8 line decoder

In Enter Program into Trainer Kit

1. Press 'RESET' key
2. Sub (key processor represent address field)
3. Enter the address (16 bit) and digit in hex

4. Press ‘NEXT’ key
5. Enter the data
6. Again press “NEXT”
7. Again after taking the program, are use HLT instruction its Hex code
8. Press “NEXT”

How to executive program

1. Press “RESET”
2. Press “GO”
3. Enter the address location in which line program was executed
4. Press “Execute” key

RESULT

Thus 8085 microprocessor was studied successfully.

PRECAUTIONS

1. Connections should be proper and tight.
2. Switch “ON” the power after completing the circuit.